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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/505,192	02/16/2000	Yoshiharu Hashimoto	Q57919	6549

7590 06/18/2002

MACPEAK & SEAS
2100 Pennsylvania Avenue NW
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EXAMINER
NGUYEN, KEVIN M

ART UNIT	PAPER NUMBER
2674	

DATE MAILED: 06/18/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/505,192	Applicant(s) HASHIMOTO, YOSHIHARU
	Examiner Kevin M. Nguyen	Art Unit 2674

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 April 2002* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-4 and 6-8* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4 and 6-8* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

1. The amendment filed on 4/3/2002 is entered. The rejections of claims 1-4 and 6-8 are maintained.

Drawings

2. The corrected or substitute drawings were received on 4/3/2002. These drawings are acknowledged and approved.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1-4 and 6-8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's Admitted Prior Art hereinafter AAPA in view of Yanagi et al (US 5,929,847).

5. As to claim 1, AAPA discloses the conventional driving circuit having data 6 bits, a gray shade voltage generating circuit 56 which is used to divide gray shade voltage including 9 voltage values from V0 to V8, a gray shade voltage selecting circuit 54 is used to select one voltage out of a plurality of voltages supplied from a grayscale voltage generating circuit 56 in accordance with D00-D05 (6 high bit order). When the digital data image D00-D05 is transferred to the data latch circuit 53, one grayscale is selected based on the digital data image D00-D05 (6 high bit order) that composed of at least one bit from the most significant bit of which is satisfied one bit is smaller than 6

high bit order and for output the voltage (see figure 11, page 2, lines 4-19). AAPA teaches a amplifier 55 (figure 11), but AAPA fails to teach "voltage adjusting means for inducing a voltage rise or a voltage drop of the voltage outputted from said operational amplifier based on low bits of said digital image data excluding said high order bits." However, Yanagi teaches the related grayscale voltage generating circuit having the operational amplifier Opy and Opz to adjust the potential high Vhigh and the potential low Vlow to the pulse voltage Vy (high) and the pulse voltage Vz (low) in accordance with the pulse POL (one lower order bit) go high level and low level (see figure 10 and figure 11, col. 26, lines 1-29). It would have been obvious to a person of ordinary skill in the art at the time of the invention to utilize the functionality of the operational amplifier circuit taught by Yanagi in AAPA's operational amplifier in order to amplifier the grayscale voltage signal because it is noted that the present invention can be applied to the conventional driver circuit for a display panel (see col. 40, lines 44-45 of Yanagi).

6. As to claim 2, Yanagi teaches, referring to Fig. 17, the voltage generating circuit having the operational amplifier (op-amp) OPa, a resistor R3 connected at node Vy and source of transistor SW1, a signal POL (one order bit), a level conversion circuit 2 (control means) (see col. 30, lines 55-67).

7. As to claim 3, Yanagi teaches, referring to Fig. 17, two transistors SW1 and SW2 connecting to a resistor R3 and a level conversion circuit 2, the level conversion circuit 2 converting the signal POL (one order bit).

8. As to claim 4, Yanagi teaches, referring to Fig. 17, the resistor R3 including the capacitor Cy (an analog switch).

9. As to claim 6, AAPA discloses the gray shade voltage of 9 values inputted from outside are divided to generate the gray shade voltage of 64 values such as a voltage divider method or resistance string method (see page 2, lines 20-23).

10. As to claim 7, Yanagi teaches, referring to Fig. 19, the amplitude can be adjusted with the control voltage Vac and the center of the amplitude can be adjusted with the control voltage Vdc (see col. 31, lines 1-11).

11. As to claim 8, Yanagi teaches digital image signal (see table 2, col. 19, lines 15-26), for example 1110 1011_2, 8 bits (N), high order bit or most significant bit is the leftmost digit; the rightmost is the low-order or least significant digit.

Response to Arguments

12. Applicant's arguments filed 4/3/2002 have been fully considered but they are not persuasive.

In response to applicant's argument that claim 1 recites "grayshade voltage selecting means for selecting one voltage out of a plurality of voltages supplied from a grayshade voltage generating means based on high order bits composed of at least one bit counted from the most significant bit of a digital image data and the number of bits of which is smaller than that of the digital image data, and for outputting a voltage..... excluding a high order bits." This argument is not persuasive because AAPA discloses the conventional driving circuit having data 6 bits, a gray shade voltage generating circuit 56 which is used to divide gray shade voltage including 9 voltage values from V0 to V8, a gray shade voltage selecting circuit 54 is used to select one voltage out of a plurality of voltages supplied from a grayscale voltage generating circuit 56 in

accordance with D00-D05 (6 high bit order). When the digital data image D00-D05 is transferred to the data latch circuit 53, one grayscale is selected based on the digital data image D00-D05 (6 high bit order) that composed of at least one bit from the most significant bit of which is satified one bit is smaller than 6 high bit order and for output the voltage (see figure 11, page 2, lines 4-19). AAPA teaches a amplifier 55 (figure 11), but AAPA fails to teach "voltage adjusting means for inducing a voltage rise or a voltage drop of the voltage outputted from said operational amplifier based on low bits of said digital image data excluding said high order bits." These argument are not persuasive because Yanagi's invention teaches the related grayscale voltage generating circuit having the operational amplifier Opy and Opz to adjust the potential high Vhigh and the potential low Vlow to the pulse voltage Vy (high) and the pulse voltage Vz (low) in accordance with the pulse POL (one lower order bit) go high level and low level (see figure 10 and figure 11, col. 26, lines 1-29). Examiner disagrees with Applicant's position that Yanagi does not teach relate to grayscale display. One skill in the art to recognize that Yanagi does teach a relate grayscale display device (see figure 10 and figure 11, col. 26, lines 1-29) to utilize the functionality of the operational amplifier circuit taught by Yanagi in AAPA's operational amplifier in order to amplifier the grayscale voltage signal because it is noted that the present invention can be applied to the conventional driver circuit for a display panel (see col. 40, lines 44-45 of Yanagi). See the attachment for explanation of most significant bit and least significant bit.

For these reasons, the rejections based on AAPA and Yanagi have been maintained.

Conclusion

13. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

1. Any inquiry concerning this communication or earlier communications from the examiner should be directed to **Kevin M. Nguyen** whose telephone number is **703-305-6209**. The examiner can normally be reached on MON-FRI from 9:00-5:00 with alternate Friday off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, **Richard A Hjerpe** can be reached on **703-305-4709**.

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks

Washington, D.C. 20231

or faxed to:

(703) 872-9314 (for Technology Center 2600 only)

Hand-delivered response should be brought to Crystal Park II, 2121 Crystal Drive, Arlington, VA, Sixth floor (Receptionist).

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Technology Center 2600 Customer Service Office whose telephone number is (703) 306-0377.

Kevin M. Nguyen
Examiner
Art Unit 2674

RICHARD HJERPE
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2600